REMARKS

Claims 17–23, 25, 46–49 and 51–59 are pending in the present application.

Claims 46-49 and 51-57 are rejected.

Claims 17–23, 25, 58 and 59 are withdrawn from consideration.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 102 (Anticipation)

Claims 46, 48–49, 51–52 and 54–55 were rejected under 35 U.S.C. § 102(b) as being anticipated by "Fabrication Technique for Fully Recessed Oxide Isolation," IBM Technical Disclosure Bulletin vol. 19, no. 10, pp. 3947-3950 (March 1, 1977) ("the IBM TDB"). These rejections are respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-76 (8th ed. rev. 3 August 2005).

Independent claims 46 recites an uplift in portions of the nitride layer proximate to the peripheral edge caused by reoxidation of the gate structure to eliminate asperities from the polysilicon. Such a feature is not found in the cited reference.

The specification of the present application teaches that asperities on the bottom of the polysilicon layer within polysilicon gate electrodes led to the discontinuance of reoxidation of the

polysilicon gate electrodes (and etching of the oxides formed on the sidewalls of the polysilicon during such reoxidation) for small geometry devices:

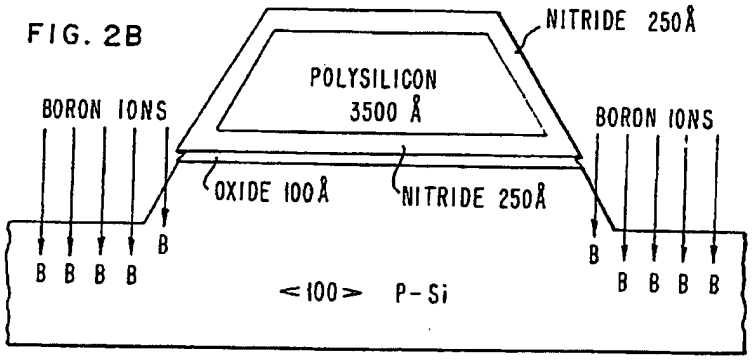
> In manufacturing transistors, re-oxidation has been used in 5 μm to 1.2 μm technologies to improve transistor lifetimes and gate oxide reliability due to higher fields occurring at the etched polysilicon transistor edges. For example, U.S. Pat. No. 4,553,314 teaches using re-oxidation to manufacture semiconductor devices. Typically, 3 μm and 5 μm technologies use re-oxidation thicknesses from about 1200 Å to about 2500 Å depending on the particular device. In 1.5 μm and 2 μm technologies, re-oxidation thicknesses from about 500 Å to about 1,000 Å are used.
>
> In 0.8 μm technology, however, the re-oxidation process has been discontinued because the lifetimes of transistors currently manufactured without the re-oxidation process is better than with the re-oxidation process. Such a situation is caused by the formation of asperities on the underside of the polysilicon layer of the transistor during the re-oxidation process. These asperities are of little importance until the gate oxide thicknesses are reduced to below 200 Å as used in submicron technology. At this point, the asperities become a contributor to the increased field at the transistor edge and of hot carrier injection (HCI). These asperities are caused by (1) oxidant diffusion along polysilicon grain boundaries creating single crystal silicon protrusions and (2) oxide thicknesses under the polysilicon edge increasing during re-oxidation, causing polysilicon grain boundary slip to occur and creating multiple edges, which results in an overall increase in angle geometries.

Specification, page 2, line 8 through page 3, line 2. The present invention teaches that reoxidation of polysilicon gate electrodes – without the normally attendant problem of asperities – is possible if a silicon nitride layer is formed beneath the polysilicon:

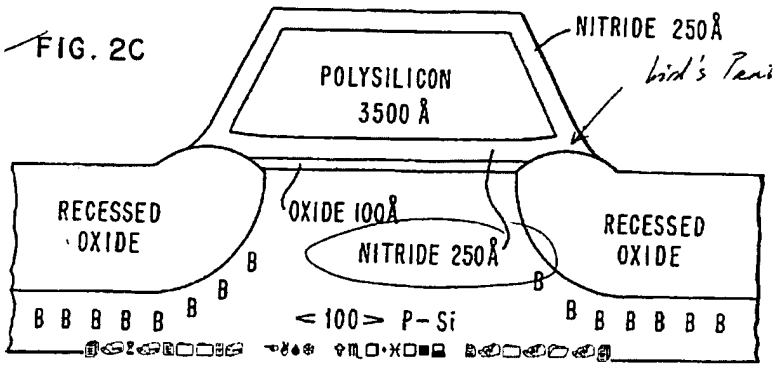
> The present invention allows for the use of re-oxidation to improve transistor lifetimes by reducing fields in transistor technologies through elimination of previous limitations. According to the present invention, a structure is provided which uses the increased distance at the gate edge, but eliminates the asperities created during re-oxidation so that re-oxidation may be used for submicron technologies. The structure of the present invention prevents the effects of oxidation on the polysilicon gate by using a thin silicon nitride layer located between the polysilicon and the gate oxide in a transistor.

Specification, page 6, lines 13–24. During reoxidation of the polysilicon gate electrode, however, the peripheral edges of the nitride layer are lifted. Independent claim 46 thus reads on the structure of an integrated circuit after the polysilicon gate electrode has been reoxidized, and the resulting oxide on the sidewalls of the polysilicon layer removed to improve transistor lifetimes and gate oxide reliability due to higher electric fields at the etched-back polysilicon layer edges.

The IBM TDB does NOT teach reoxidation of a polysilicon gate structure (with or without subsequent removal of the oxide formed on the polysilicon sidewalls during reoxidation). In the IBM TDB, the polysilicon is completely encased in nitride and cannot be reoxidized:



Moreover, it is apparent from the IBM TDB that the lift in peripheral regions of the silicon nitride encasing the polysilicon results from growth of conventional LOCOS field oxidation, NOT from reoxidation of the polysilicon:



While both LOCOS field oxidation and reoxidation result in lift of peripheral regions of the nitride layer, only reoxidation of the polysilicon gate electrode results in the structure and benefits of a reoxidized polysilicon layer, without asperities on the bottom of the polysilicon layer as recited in the claim. The Office Action's dismissal of reoxidation as merely a method of forming the structure is improper, because reoxidation changes the structure and nature of the polysilicon layer, resulting in a different structure and different operating characteristics than simple deposited polysilicon. By way of analogy, vulcanized rubber is materially different as a substance or structure than non-vulcanized rubber, despite the fact that the adjective "vulcanized" specifies a process performed on the basic rubber material to form vulcanized rubber.

Therefore, the rejection of claim 46, 48–49 and 51–55 under 35 U.S.C. § 102 has been overcome.

35 U.S.C. § 103 (Obviousness)

Claims 46–49, 52–53 and 55–57 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,192,059 to *Khan et al* in view of the IBM TDB. This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 3 August 2005). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

As noted above, independent claim 46 recites a feature not found in the IBM TDB. Similarly, such a feature is not found in *Khan et al*. *Khan et al* does not teach reoxidation of the entire gate structure, such as would cause an uplift in peripheral portions of the nitride 5 and eliminate asperities

on the bottom of polysilicon 15, but instead teaches growing oxide only on an upper surface of the polysilicon layer 15.

Therefore, the rejection of claims 46–49, 52–53 and 55–57 under 35 U.S.C. § 103 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: 3-1-06

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